PATENT
Attorney Docket No.: 213.302
Express Mail Label No.: EL662348256US

Sequencer and Method of Selectively Inhibiting Clock Signals to Execute Reduced Instruction Sequences in a Re-Programmable I/O Interface

Cross-reference to Related Invention

This invention is related to an invention for a "Dual-Edge Function Clock Generator and Method of Deriving Clocking Signals for Executing Reduced Instruction Sequences in a Re-Programmable I/O Interface," described in U.S. Patent application ~~Serial~~ No. 6,664,833 (~~SE-1588/213.301~~), filed concurrently herewith by the present inventor and assigned to the assignee hereof. The disclosure of this concurrently filed application is incorporated herein by this reference.

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Field of the Invention

This invention relates to input/output (I/O) interfaces used for connecting relatively complex and high capacity computer systems to peripheral equipment. More particularly, the present invention relates to a new and improved I/O interface by which to send and receive communication signals, preferably in a serial or narrow parallel form, which offers the advantage of relatively small size, relatively high performance, relatively low power consumption, and comparatively great versatility and flexibility in accommodating and executing a variety of different complex communication protocols.

Background of the Invention

Many modern electronic devices are built as an entire system on a single semiconductor chip, and as such, are known as system on a chip (SoC) integrated circuits or application specific standard products (ASSPs). Building an entire system or large portion of the system on a single chip has a number of advantages. Although the costs of initially designing and fabricating the component may be relatively high, it is very inexpensive to replicate large numbers of the systems, thereby reducing the cost of the system on a per unit basis. By designing the entire system or large portion of the system on a single chip, a high level of functionality